CLAIMS

1. A method for manufacturing an integrated circuit, the method comprising:

(a) forming a plurality of first conductive gates for nonvolatile memory cells, the first conductive gates being spaced from each other and not electrically interconnected;

(b) forming a plurality of conductive floating gates for the memory cells;

(c) forming a plurality of second conductive gates for the memory cells;

(d) forming at least one conductive line electrically interconnecting two or more of the first conductive gates.

2. The method of Claim 1 wherein the first conductive gates are formed before the floating gates and the second conductive gates.

3. The method of Claim 2 wherein the conductive line is formed after the first conductive gates, the floating gates, and the second conductive gates.

4. The method of Claim 1 wherein the conductive line is formed after the first conductive gates, the floating gates, and the second conductive gates.

5. The method of Claim 1 further comprising, after forming the first conductive gates and at least one of the floating gates and the second conductive gates, forming a dielectric to insulate the at least one of the floating gates and the second conductive gates from the conductive line, wherein the dielectric is at least 200 Å thick.

6. The method of Claim 5 wherein the dielectric is at least 500 Å thick.

7. The method of Claim 1 wherein the first conductive gates comprise a semiconductor material, and the conductive line is a metal line.

8. The method of Claim 1 wherein the operation (c) comprises forming at least one conductive line which provides the second conductive gates to at least two adjacent columns of the memory cells.

9. The method of Claim 8 wherein each conductive line formed in the operation (d) interconnects the first conductive gates for at least one row of the memory cells.

10. The method of Claim 1 wherein a plurality of the second conductive gates are interconnected by a conductive line perpendicular to the conductive lines formed in the operation (d).

11. The method of Claim 1 further comprising forming substrate isolation regions in the semiconductor substrate between active areas of the semiconductor substrate, each substrate isolation region being a dielectric region protruding above the semiconductor substrate;

wherein the operation (a) comprises forming first gate structures protruding above the semiconductor substrate, each first gate structure overlying at least one active area, wherein each first gate structure comprises one of the first conductive gates;

wherein the operation (b) comprises:

(b1) forming a conformal layer ("FG layer") over the first gate structures and the substrate isolation regions, wherein each floating gate comprises a portion of the FG layer, wherein a maximum distance between points of the adjacent substrate isolation regions above the substrate is not greater than one half of a thickness of the FG layer, and one half of the thickness of the FG layer is smaller than a distance between the adjacent first gate structures; and

(b2) isotropically etching the FG layer to expose the substrate isolation regions and to remove the FG layer from over at least a portion of each first gate structure.

12. The method of Claim 1 further comprising forming substrate isolation regions in the semiconductor substrate between active areas of the semiconductor substrate, each substrate isolation region being a dielectric region protruding above the semiconductor substrate;

wherein the operation (a) comprises forming first gate structures protruding above the semiconductor substrate, each first gate structure overlying at least one active area, wherein each first gate structure comprises one of the first conductive gates;

wherein the operation (b) comprises:

(b1) forming a conformal layer ("FG layer") over the first gate structures and the substrate isolation regions, wherein each floating gate comprises a portion of the FG

layer, wherein the FG layer comprises a planar area between each two adjacent substrate isolation regions and the FG layer comprises a protrusion over each first gate structure; and

(b2) isotropically etching the FG layer to expose the substrate isolation regions and to remove the FG layer from over at least a portion of each first gate structure.

13. An integrated circuit comprising:

a plurality of first conductive gate structures, each first conductive gate structure comprising a first conductive gate of a nonvolatile memory cell, the first conductive gate structures being spaced from each other, the first conductive gates comprising a semiconductor material;

a plurality of conductive floating gates for the memory cells;

a plurality of second conductive gates for the memory cells;

at least one metal line physically contacting two or more of the first conductive gate structures to electrically interconnect the respective two or more first conductive gates.

14. The integrated circuit of Claim 13 further comprising a dielectric overlying the floating gates and the second conductive gates and underlying the metal line.

15. The integrated circuit of Claim 14 wherein the dielectric is at least 200 Å thick.

16. The integrated circuit of Claim 14 wherein the dielectric is at least 500 Å thick.

17. The integrated circuit of Claim 13 comprising at least one conductive line which provides the second conductive gates to at least two adjacent columns of the memory cells.

18. The integrated circuit of Claim 17 wherein each metal line electrically interconnects the first conductive gates for at least one row of the memory cells.

19. The integrated circuit of Claim 13 comprising a semiconductor substrate, wherein each memory cell comprises a channel area underlying a floating gate and a channel area underlying a first conductive gate.

20. The integrated circuit of Claim 19 wherein each memory cell comprises two floating gates and two channel areas underlying the two floating gates.

21. The integrated circuit of Claim 13 wherein a plurality of the second conductive gates are interconnected by a conductive line perpendicular to the metal line.

22. An integrated circuit comprising:

a plurality of first conductive gate structures, each first conductive gate structure comprising a first conductive gate of a nonvolatile memory cell, the first conductive gate structures being spaced from each other;

a plurality of conductive floating gates for the memory cells;

a plurality of second conductive gates for the memory cells;

a dielectric overlying the floating gates and the second conductive gates;

at least one conductive line overlying the dielectric and physically contacting two or more of the first conductive gate structures;

wherein the dielectric is at least 200 Å thick.

23. The integrated circuit of Claim 22 wherein the dielectric is at least 500 Å thick.

24. The integrated circuit of Claim 22 comprising at least one conductive line which provides the second conductive gates to at least two adjacent columns of the memory cells.

25. The integrated circuit of Claim 22 comprising a semiconductor substrate, wherein each memory cell comprises a channel area underlying a floating gate and a channel area underlying a first conductive gate.

26. The integrated circuit of Claim 25 wherein each memory cell comprises two floating gates and two channel areas underlying the two floating gates.

27. The integrated circuit of Claim 22 wherein a plurality of the second conductive gates are interconnected by a conductive line perpendicular to the conductive line contacting the first conductive gate structures.

28. A method for fabricating an integrated circuit which comprises nonvolatile memory cells, each memory cell having a conductive floating gate and a first conductive gate insulated from each other, the method comprising:

(a) forming substrate isolation regions in a semiconductor substrate between active areas of the semiconductor substrate, each substrate isolation region being a dielectric region protruding above the semiconductor substrate;

(b) forming first gate structures protruding above the semiconductor substrate, each first gate structure overlying at least one active area, wherein each first gate structure comprising at least one first conductive gate;

(c) forming a conformal layer ("FG layer") over the first gate structures and the substrate isolation regions, wherein each floating gate comprises a portion of the FG layer, wherein a maximum distance between points of the adjacent substrate isolation regions above the substrate is not greater than one half of a thickness of the FG layer, and one half of the thickness of the FG layer is smaller than a distance between the adjacent first gate structures;

(d) isotropically etching the FG layer to expose the substrate isolation regions and to remove the FG layer from over at least a portion of each first gate structure.

29. The method of Claim 28 wherein the operation (d) is terminated with reference to a time of detecting that the substrate isolation regions have been exposed.

30. The method of Claim 28 wherein each substrate isolation region traverses an array of the memory cells.

31. The method of Claim 28 wherein first gate structures comprise a dielectric over sidewalls of first conductive gates to insulate the first conductive gates from the floating gates.

32. The method of Claim 28 wherein each memory cell further comprises a second conductive gate insulated from the first conductive gate and the floating gate.

33. A method for fabricating an integrated circuit which comprises nonvolatile memory cells, each memory cell having a conductive floating gate and a first conductive gate insulated from each other, the method comprising:

(a) forming substrate isolation regions in a semiconductor substrate between active areas of the semiconductor substrate, each substrate isolation region being a dielectric region protruding above the semiconductor substrate;

(b) forming first gate structures protruding above the semiconductor substrate, each first gate structure overlying at least one active area, wherein each first gate structure comprising at least one first conductive gate;

(c) forming a conformal layer ("FG layer") over the first gate structures and the substrate isolation regions, wherein each floating gate comprises a portion of the FG layer, wherein the FG layer comprises a planar area between each two adjacent substrate isolation regions and the FG layer comprises a protrusion over each first gate structure; and

(d) isotropically etching the FG layer to expose the substrate isolation regions and to remove the FG layer from over at least a portion of each first gate structure.

34. The method of Claim 33 wherein the operation (d) is terminated with reference to a time of detecting that the substrate isolation regions have been exposed.

35. The method of Claim 33 wherein each substrate isolation region traverses an array of the memory cells.

36. The method of Claim 33 wherein first gate structures comprise a dielectric over sidewalls of first conductive gates to insulate the first conductive gates from the floating gates.

37. The method of Claim 33 wherein each memory cell further comprises a second conductive gate insulated from the first conductive gate and the floating gate.